REMARKS

In response to the Office Action mailed March 9, 2007, Applicants respectfully request reconsideration of the Application in view of the foregoing Amendments and the following Remarks. The claims as now presented are believed to be in allowable condition.

Claims 1 and 11 have been amended. Claims 1-20 remain in this application, of which claims 1 and 11 are independent claims.

Rejection of Claims 1-5, 7-9, 11-15, and 17-19 under 35 U.S.C. §103(a)

Claims 1-5, 7-9, 11-15, and 17-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,883,844 to So (hereafter referred to as "So") in view of U.S. Patent No. 6,308,249 to Okazawa (hereafter referred to as "Okazawa"). Applicants respectfully traverse this rejection.

I. The Prior Art Must be Considered in Its Entirety

§2141.02, VI of the MPEP states:

> **VI. PRIOR ART MUST BE CONSIDERED IN ITS ENTIRETY, INCLUDING DISCLOSURES THAT TEACH AWAY FROM THE CLAIMS**
> A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention.

In contradiction to such a fundamental tenet, the Examiner just takes a piece-meal disclosure of stressing only two adjacent rows R and only two adjacent columns of the memory block in So. For example, the Examiner on page 12, paragraph 22 of the Office Action dated March 9, 2007 states:

> ...As first cited in the Office action dated October 23, 2006 as well as in the present Office action above, the Examiner has stated that the boundaries between only two adjacent rows R and only two adjacent columns C of the memory block (i.e., the ***selected portion*** of memory) are analogous to the Applicant's memory device. Thus,

> Applicant is reminded that the ***Examiner is relying on So's selected portion of memory to teach Applicant's memory device***. Therefore, when taking this selected portion of memory into consideration, even though So may teach stressing and testing only a very small portion of the memory block (i.e., the selected portion of memory), it follows that all possible row and column addresses of the row and column address bits still fall within the boundaries of this selected portion of memory. As cited above, So applies the test pattern across the entire selected portion of memory. Accordingly, So sufficiently discloses each of all possible row and column addresses of the row and column address bits is cycled through for application of the stressing signals. (Emphasis added.)

Firstly, please note that the Examiner is in error in terms of his understanding of technology because if just two adjacent rows and columns of the memory block are stressed in So, then ***all*** possible row and column addresses of ***all of*** the row and column address bits for indicating just such two adjacent rows and columns would not have the stressing voltages applied thereon.

All of the row and column address bits are used for specifying much more numerous rows and columns for the whole memory block than just the selected two adjacent row and column addresses that have the stressing voltage applied thereon in So.

Generally, one of ordinary skill in the art knows that ***a whole "memory block"*** comprises all possible addresses of ***all of*** the row and column address bits, ***which are much more numerous than just the two selected adjacent rows and columns addresses of So***.

Secondly, the Examiner completely ignores the numerous portions of So that ***strongly and repeatedly teach away*** from the limitation of cycling through ***all possible*** row and column addresses of the ***all of*** the row and column address bits. Applicants hereby list the numerous instances of So with such a teaching away as completely ignored by the Examiner:

(1) The Abstract of So states:

> ....The integrated circuit also includes a selectable stress tester on the substrate and connected to the memory block for ***selectively stress testing only portions*** of the memory

block ***and not other portions*** so as to determine whether to accept or reject a memory block. (Emphasis added.)

(2) Col. 2, lines 27-67 of So states:

> With the foregoing in mind, the present invention advantageously provides a method of stress testing an integrated circuit having memory and an integrated circuit having stress testing for memory of the integrated circuit which ***significantly reduces the amount of time*** required to test the memory....
>
> ....
>
> ....Selectable stress testing means is formed on the substrate and is connected to the memory block for selectively stress testing ***only selected portions*** of the memory block ***and not others*** so as to determine whether to accept or reject a memory block. (Emphasis added.)

(3) Col. 5, lines 3-27 of So states:

> ....for selectively stress testing only portions of the memory block 20 and not other portions for a ***concentrated predetermined period of time*** so as to determine to whether to accept or reject the memory block 20.
>
> ....
>
> ....***only selected potentially weak areas*** of a memory block 20 need be tested to thereby statistically predict whether to accept or reject the memory block 20 based upon the results of the test. These selected areas, for example, are preferably weak areas across boundary lines preferably between side-by-side columns and/or side-by-side rows....

Such text are just a few examples of the more numerous portions of So that tout the advantage of ***reducing testing time*** by testing only a very small portion of the selected weak areas such as just two adjacent rows and columns of the memory block. The smaller the area to be stress tested, the more the test time may be reduced in So.

Thus, by touting the advantage of reducing testing time, So ***strongly and repeatedly*** teaches away from cycling through all possible row and column addresses of ***all of*** the row and column address bits for applying the stress voltages.

The Examiner is respectfully reminded that §2141.02, VI of the MPEP states the fundamental tenet that the ***whole*** reference of So must be considered in its ***entirety***, especially for any portions of So that would teach away from the claimed invention.

II. The Proposed Modification Cannot Render the Prior Art Unsatisfactory for its Intended Purpose

§2143.01, V of the MPEP states:

> **V. THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART UNSATISFACTORY FOR ITS INTENDED PURPOSE**
> If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.

As shown by the above-cited text of So, the intended purpose of So is to reduce testing time by stress testing only the very small selected weak area of the memory block. If So were to be modified to having ***all possible*** row and column addresses of ***all of*** the row and address bits stress tested, then the test time would increase.

Thus, modification of So to the present invention would be completely against the intended purpose of reducing testing time in So. This is because the intended purpose of So (i.e., minimizing test time) is completely different from the intended purpose of the present invention (i.e., minimizing charge gain failure).

III. No Prima Facie Case of Obviousness

The rejection of claims 1 and 11 under 35 U.S.C. §103(a) as being unpatentable over So in view of Okazawa is not appropriate because claims 1 and 11 have been amended, and a prima facie case of obviousness cannot be established for such amended claims.

In giving an obviousness rejection, the Examiner bears the initial burden of factually supporting a prima facie conclusion of obviousness. (See, MPEP, §2142). To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be ***some suggestion or motivation***, either in the references themselves or in the knowledge generally available to one

of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, ***the prior art references*** must teach or suggest ***all the claim limitations***. (See, MPEP, §2142.) (Emphasis added.)

The rejection of amended claims 1 and 11 under 35 U.S.C. §103(a) as being unpatentable over So in view of Okazawa is not appropriate because *inter alia* these prior art references fail to teach or suggest all the claim limitations and because there is no motivation or suggestion in these references to combine or modify these references to the present invention.

Amended claims 1 and 11 recite that the predetermined number of bits for each address includes row and column address bits with each of ***all possible*** row and column addresses of ***all of*** the row and column address bits being cycled through for the application of the stressing signals.

For example, the Present Application at page 6, line 20 to page 7, line 2 describes address bits A[20:0] including row address bits A[15:7] and column address bits A[6:0]. In addition, the Present Application clearly describes cycling through all possible addresses with all of the address bits A[20:0].

In contrast, So clearly teaches away from such a limitation by repeatedly touting testing only a extremely small portion of the memory block for reducing test time as stated at col. 1, line 66 to col. 2, line 67 of So:

> ....Some conventional parallel test operations can continue to take ***extensive amounts of time*** to accomplish the testing results.
>
> ....
>
> ....A method preferably includes generating a high frequency waveform signal and generating a test pattern across boundaries ***between only two columns and only two rows*** of the memory block, i.e., preferably adjacent columns and adjacent rows, responsive to the high frequency waveform signal so as to determine whether to accept or reject the memory block. (Emphasis Added.)

Repeatedly, col. 5, lines 3-27 of So states:

> ....for selectively stress testing ***only portions of the memory block*** 20 and not other portions for a concentrated predetermined period of time so as to determine to whether to accept or reject the memory block 20...
>
> ....***only selected potentially weak areas of a memory block*** need be tested to thereby statistically predict whether to accept or reject the memory block 20 based upon the results of the test. These selected areas, for example, are preferably weak areas across boundary lines preferably between side-by-side columns and/or side-by-side rows. (Emphasis Added.)

Thus, the main purpose of So is to test only a very small portion (only two rows and two columns) of the memory block for minimizing test time.

Generally, one of ordinary skill in the art knows that ***a whole "memory block"*** is comprised of all possible addresses of all of the row and column address bits, ***which are much more numerous than just the two selected adjacent rows and columns addresses of So.***

So repeatedly touts minimizing test time by stressing and testing only a very small portion of the memory block (such as two rows and two columns when a memory block typically has tens of thousands of row and columns).

Thus, So ***strongly teaches away*** from the limitation of cycling through each of ***all possible*** row and column addresses of ***all of*** the row and column address bits for the application of the stressing signals, as recited in amended claims 1 and 11.

Okazawa simply discloses typical read/write access of a memory device within a general computer system using gray code address sequencing for minimizing power consumption. Okazawa no where even remotely mentions any stress testing of any memory device.

In addition, for typical read/write access of the memory device in the general computer system of Okazawa, just the selected row and column addresses of the memory device associated with data to be processed would be sequenced. ***Thus, all possible row and column addresses of***

the memory device would be not cycled through for typical read and write accessing of the memory device in Okazawa.

Thus, So and/or Okazawa, ***either individually or in combination*** do not disclose, teach, or suggest cycling through each of ***all possible*** row and column addresses of ***all of*** the row and column address bits for the application of the stressing signals. In fact, So repeatedly and strongly teaches away from such a limitation by touting minimization of test time by stressing and testing only a very small portion of the memory block.

Accordingly, a prima facie conclusion of obviousness of claims 1 and 11 cannot be established because So and/or Okazawa fail to suggest or motivate all the claim limitations of claims 1 and 11, and the rejection of claims 1 and 11 under 35 U.S.C. §103(a) should be withdrawn.

Claims 2-5 and 7-9, which depend from and further limit claim 1, are allowable for at least the same reasons that claim 1 is allowable as stated above.

Claims 12-15 and 17-19, which depend from and further limit claim 11, are allowable for at least the same reasons that claim 11 is allowable as stated above.

Rejection of Claims 6, 10, 16, and 20 under 35 U.S.C. §103(a)

Claims 6 and 10, which depend from and further limit claim 1, are allowable for at least the same reasons that claim 1 is allowable as stated above.

Claims 16 and 20, which depend from and further limit claim 11, are allowable for at least the same reasons that claim 11 is allowable as stated above.

Conclusions

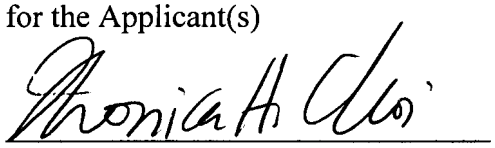
In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested.

If the Examiner still disagrees, a timely Office Action made Final is requested to be sent ASAP such that an Appeal may be filed soon.

Please feel free to contact the undersigned should any questions arise with respect to this case that may be addressed by telephone.

Respectfully submitted,
for the Applicant(s)

Dated: May 24, 2007

By: 

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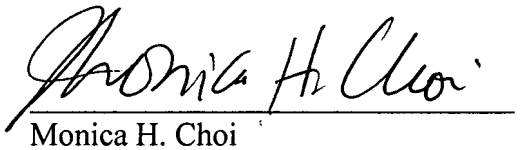
CERTIFICATE OF MAILING

The undersigned hereby certifies that the foregoing AMENDMENT AND RESPONSE is being deposited in the United States Postal Service, as first class mail, postage prepaid, in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 24th day of May, 2007.



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